IN THE SPECIFICATION

Please amend paragraph [0004] as follows:

[0004] Building computer logic takes many steps before the computer logic is physically manufactured. The logic designer typically uses synthesis tools, known as Hardware Descriptor Languages (HDLs), to describe, design and document electronic circuits, as well as simulating faults, in software simulations of hardware. Examples of HDLs are [[Verilog®]] VERILOG® and VHDL (Very-high-speed-integrated-circuit Hardware Descriptor Language) for Very Large Scale Integrated Circuits (VLSICs); and Register Transfer Language (RTL) to describe registers in computer logic and the way that data is transferred between such registers. By including a description of interfaces for logic and the logic's behavior, HDLs simulate physical hardware to such an extent that a virtual machine can be constructed in software alone. Such virtual machines are made up of multiple Finite State Machines (FSMs), also referred to as function areas or logic areas. Examples of FSMs are error correction logic, arbitration units, flow-control management units for determining if packets can be sent, etc.

Please amend paragraph [0014] as follows:

[0014] [[Figure 5 illustrates]] Figures 5a-b illustrate which test cases fail after altering a logic area;